Abstracts

CMOS layout and bias optimization for RF IC design applications

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High frequency and low noise performance of 0.8 /spl mu/m polysilicon gate CMOS device has been analyzed intensively with the various multi-finger polysilicon gate layout and bias to find the optimal condition. From the analysis, the optimal width of unit gate finger and bias condition have been found to maximize f/sub max/ and minimize F/sub min/. At the conditions, F/sub min/, gain and noise resistance characteristics of large width transistors are also analyzed.

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